REMARKS

This paper is responsive to a Non-Final Office action dated June 2, 2006. Claims 1-25 were examined. Claims 1-7, 11, 15-17, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,118,316 to Tamamura in view of U.S. Patent No. 6,959,062 to Stubbs. Claims 10, 12, 13, 18, 19, 22, 23, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tamamura in view of Stubbs and U.S. Patent No. 6,711,227 to Kaylani et al. Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tamamura in view of Stubbs and U.S. Patent No. 6,118,316 to Bulzachelli. Claims 8 and 9 are allowed. Claims 20 and 21 are objected to as being dependent upon a rejected base claim.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-7, 11, 15-17, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,118,316 to Tamamura (hereinafter, "Tamamura") in view of U.S. Patent No. 6,959,062 to Stubbs (hereinafter, "Stubbs").

Regarding claim 1, Applicants respectfully maintain that Tamamura, alone or in combination with Stubbs or other references of record, fails to teach or suggest

> a phase detector circuit coupled to generate a difference signal indicating a phase difference between an incoming data stream and a delayed clock signal and a clock delay circuit coupled to receive a delay control signal derived from the difference signal and to receive the output clock signal, the clock delay circuit coupled to provide as the delayed clock signal the output clock signal delayed according to the delay control signal,

as required by claim 1. Tamamura teaches PLL 20A that divides an oscillation output signal 203a-1 by a division ratio in divider 204-1. Col. 8, lines 64-66; Fig. 4. Tamamura teaches that a divided signal 204a-1 is compared with input data 11-1 according to frequency and phase. Col. 8, line 66-col. 9, line 1; Fig. 4. The Office Action admits that Tamamura fails to teach or suggest

a clock delay circuit receiving a delay control signal derived from the difference signal and to receive an output clock signal, the clock delay circuit coupled to provide as a delayed clock signal the output clock signal delayed according to the delay control signal. The Office Action relies on variable delay line 108 of Stubbs to supply this teaching.

Stubbs teaches that

> [v]ariable delay line 108 eceives E_CLOCK on node 104, and subjects E_CLOCK to further delay to generate the internal clock on node 110. The internal clock on node 110 is used internal to integrated circuit 100. In some embodiments, such as the embodiment shown in FIG. 1, the internal clock is fanned out to device elements within the integrated circuit. Device element 112 is representative of many possible device elements within integrated circuit 100, and can be any type of circuit element that uses the internal clock. Examples include, but are not limited to, flip-flops, latches, output registers, and output buffers. Device element 112 receives the internal clock on control input node 114. Control input node 114 can be a clock input, an output enable input, a data input, or the like. For example, in some embodiments, device element 112 is a flip-flop and control input node 114 is a clock input. In other embodiments, device element 112 is a buffer and control input node 114 is an output enable that switches an output from a high impedance state to a driven state.

Col. 3, lines 1-19 (emphasis added). Control signals on nodes 132 and 134 of Stubbs are based on I_CLOCK, the delayed clock signal, and E_CLOCK, which are input to phase detector 130. Fig. 1; col. 4, lines 28-42. The internal clock on node 110 of Stubbs is output from the delay locked loop to other circuitry internal to integrated circuit 100. Variable delay line 108 of Stubbs does not receive an output clock signal, as required by claim 1. Thus, variable delay line 108 of Stubbs fails to teach or suggest a clock delay circuit coupled to receive a delay control signal derived from the difference signal and to receive the output clock signal, the clock delay circuit coupled to provide as the delayed clock signal the output clock signal delayed according to the delay control signal, as required by claim 1. Nowhere does Stubbs teach or suggest the limitations of claim 1.

Thus, Applicants respectfully maintain that neither Tamamura, alone or in combination with Stubbs or other references of record, teaches or suggests the limitations of claim 1. For at least this reason, Applicants believe that claim 1 is allowable over the art of record.

Accordingly, Applicants respectfully request that the rejection of claim 1 and all claims dependent thereon, be withdrawn.

Regarding claim 15, Applicants respectfully maintain that Tamamura, alone or in combination with Stubbs or other references of record, fails to teach or suggest

> determining a phase difference between an input data stream and a delayed clock signal and generating a difference signal indicative thereof and receiving the output clock signal in a delay circuit and generating the delayed clock signal from the output clock signal according to a delay control signal derived from the difference signal,

as required by claim 15. Tamamura teaches PLL 20A that divides an oscillation output signal 203a-1 by a division ratio in divider 204-1. Col. 8, lines 64-66; Fig. 4. Tamamura teaches that a divided signal 204a-1 is compared with input data 11-1 according to frequency and phase. Col. 8, line 66-col. 9, line 1; Fig. 4. The Office Action admits that Tamamura fails to teach or suggest receiving the output clock signal in a delay circuit and generating the delayed clock signal from the output clock signal according to a delay control signal derived from the difference signal. The Office Action relies on Stubbs to supply this teaching.

Stubbs teaches that

> [v]ariable delay line 108 eceives E_CLOCK on node 104, and subjects E_CLOCK to further delay to generate the internal clock on node 110. The internal clock on node 110 is used internal to integrated circuit 100. In some embodiments, such as the embodiment shown in FIG. 1, the internal clock is fanned out to device elements within the integrated circuit. Device element 112 is representative of many possible device elements within integrated circuit 100, and can be any type of circuit element that uses the internal clock. Examples include, but are not limited to, flip-flops, latches, output registers, and output buffers. Device element 112 receives the internal clock on control input node 114. Control input node 114 can be a clock input, an output enable input, a data input, or the like. For example, in some embodiments, device element 112 is a flip-flop and control input node 114 is a clock input. In other embodiments, device element 112 is a buffer and control input node 114 is an output enable that switches an output from a high impedance state to a driven state.

Col. 3, lines 1-19 (emphasis added). Control signals on nodes 132 and 134 of Stubbs are based on I_CLOCK, the delayed clock signal, and E_CLOCK, which are input to phase detector 130. Fig. 1; col. 4, lines 28-42. The internal clock on node 110 of Stubbs is output from the delay locked loop to other circuitry internal to integrated circuit 100. Variable delay line 108 of Stubbs does not receive an output clock signal, as required by claim 15. Thus variable delay line 108 of Stubbs fails to teach or suggest receiving the output clock signal in a delay circuit and generating the delayed clock signal from the output clock signal according to a delay control signal derived from the difference signal, as required by claim 15. Nowhere does Stubbs teach or suggest the limitations of claim 15.

Thus, Applicants respectfully maintain that neither Tamamura, alone or in combination with Stubbs or other references of record, teaches or suggests the limitations of claim 15. For at least this reason, Applicants believe that claim 15 is allowable over the art of record. Accordingly, Applicants respectfully request that the rejection of claim 15 and all claims dependent thereon, be withdrawn.

Regarding claim 24, Applicants respectfully maintain that Tamamura, alone or in combination with Suzuki or other references of record fails to teach or suggest

> means for detecting a phase difference between an incoming data stream and a delayed clock signal and means for generating a control signal according to the difference signal and means for generating a clock signal that varies according to the control signal and generating a difference signal indicative thereof and means for generating the delayed clock signal from the clock signal according to a delay control signal derived from the difference signal,

as required by claim 24. Tamamura teaches PLL 20A that divides an oscillation output signal 203a-1 by a division ratio in divider 204-1. Col. 8, lines 64-66; Fig. 4. Tamamura teaches that a divided signal 204a-1 is compared with input data 11-1 according to frequency and phase. Col. 8, line 66-col. 9, line 1; Fig. 4. The Office Action admits that Tamamura fails to teach or suggest

a clock delay circuit receiving a delay control signal derived from the difference signal and to receive an output clock signal, the clock delay circuit coupled to provide as a delayed clock signal the output clock signal delayed according to the delay control signal. The Office Action relies on Stubbs to supply this teaching.

Stubbs teaches that

> [v]ariable delay line 108 eceives E_CLOCK on node 104, and subjects E_CLOCK to further delay to generate the internal clock on node 110. The internal clock on node 110 is used internal to integrated circuit 100. In some embodiments, such as the embodiment shown in FIG. 1, the internal clock is fanned out to device elements within the integrated circuit. Device element 112 is representative of many possible device elements within integrated circuit 100, and can be any type of circuit element that uses the internal clock. Examples include, but are not limited to, flip-flops, latches, output registers, and output buffers. Device element 112 receives the internal clock on control input node 114. Control input node 114 can be a clock input, an output enable input, a data input, or the like. For example, in some embodiments, device element 112 is a flip-flop and control input node 114 is a clock input. In other embodiments, device element 112 is a buffer and control input node 114 is an output enable that switches an output from a high impedance state to a driven state.

Col. 3, lines 1-19 (emphasis added). Control signals on nodes 132 and 134 of Stubbs are based on I_CLOCK, the delayed clock signal, and E_CLOCK, which are input to phase detector 130. Fig. 1; col. 4, lines 28-42. The internal clock on node 110 of Stubbs is output from the delay locked loop to other circuitry internal to integrated circuit 100. Variable delay line 108 of Stubbs does not generate the delayed clock signal from the clock signal that varies according to the control signal, as required by claim 24. Thus, variable delay line 108 of Stubbs fails to teach or suggest means for generating the delayed clock signal from the clock signal according to a delay control signal derived from the difference signal, as required by claim 24. Nowhere does Stubbs teach or suggest the limitations of claim 24.

Thus, Applicants respectfully maintain that neither Tamamura, alone or in combination with Stubbs or other references of record, teaches or suggests the limitations of claim 24. For at least this reason, Applicants believe that claim 24 is allowable over the art of record. Accordingly, Applicants respectfully request that the rejection of claim 24 and all claims dependent thereon, be withdrawn.

Claims 10, 12, 13, 18, 19, 22, 23, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tamamura in view of Stubbs and U.S. Patent No. 6,711,227 to Kaylani et al. Applicants respectfully maintain that claims 10,12, 13, 18, 19, 22, 23, and 25 depend from allowable base claims and are allowable for at least this reason.

Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tamamura in view of Stubbs and U.S. Patent No. 6,118,316 to Bulzachelli. Applicants respectfully maintain that claim 14 depends from an allowable base claim and is allowable for at least this reason.

Allowable Subject Matter

Applicants appreciate the allowance of claims 8 and 9.

Applicants appreciate the indication of allowable subject matter in claims 20 and 21. Applicants believe that claims 20 and 21 depend from allowable base claims and are allowable for at least this reason.

Although Applicants believe that claims 8, 9, 20 and 21 are allowable over the art of record, the Examiner's Reasons for Allowance do not coincide with the allowed claims. Applicants do not acquiesce in additional limitations included in the Examiner's Statement of Reasons for Allowance.

In summary, claims 1-25 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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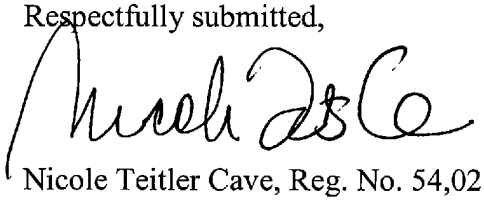

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